Paper No. 25

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

*Ex parte* TING-WAH WONG

Appeal No. 2004-0607
Application No. 09/792,848

ON BRIEF

Before OWENS, KRATZ, and TIMM, *Administrative Patent Judges*.

OWENS, *Administrative Patent Judge*.

*DECISION ON APPEAL*

This appeal is from the final rejection of claims 23-29. Claims 1-10, which are all of the other claims pending in the application, stand withdrawn from consideration by the examiner as being directed toward a nonelected invention.

*THE INVENTION*

The appellants claim an integrated circuit comprising a substrate having therein first and second triple wells, the first of which has thereover a logic circuit element and the second of which has thereover a radio frequency element. Claim 23 is illustrative:

23. An integrated circuit comprising:
a substrate;
a logic circuit element formed over said substrate;
a first triple well formed in said substrate under said logic circuit element, said triple well including a first P-well formed within a first N-well formed in said substrate, said first P-well being positioned directly beneath said logic circuit element, said first P-well being biased by a first bias potential above Vss;
a radio frequency element formed over said substrate; and
a second triple well formed under said radio frequency element, said second triple well including a second P-well directly underneath said radio frequency element and said second P-well formed in a second N-well, said first and second triple wells being isolated from one another such that said N-well of said first and second triple wells are spaced away from one another to isolate the logic circuit element from the radio frequency element, said second P-well being biased by a second bias potential above Vss.

*THE REFERENCES*

*References relied upon by the examiner*

| | | |
|---|---|---|
| Momohara | 6,055,655 | Apr. 25, 2000 |
| Zhu et al. (Zhu) | 6,133,079 | Oct. 17, 2000 |

*Reference relied upon by the appellant*

Neil H.E. Weste and Kamran Eshraghian (Weste), *Principles of CMOS VLSI Design - A Systems Perspective*" (page unknown) (Addison-Wesley 2nd ed. 1993).

*THE REJECTIONS*

The claims stand rejected as follows: claims 23-29 under 35 U.S.C. § 112, first paragraph, written description requirement; claims 23-29 under 35 U.S.C. § 103 as obvious over

Momohara; and claim 25 under 35 U.S.C. § 103 as obvious over Momohara in view of Zhu.[1]

*OPINION*

We affirm the rejection under 35 U.S.C. § 112, first paragraph, and reverse the rejections under 35 U.S.C. § 103.

*Rejection under 35 U.S.C. § 112, first paragraph*

A specification complies with the 35 U.S.C. § 112, first paragraph, written description requirement if it conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, the inventor was in possession of the invention. *See Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991); *In re Kaslow*, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983).

The appellant's claim 23, which is the sole independent claim, requires that P-wells are biased by a bias potential above Vss. No mention of Vss appears in the appellant's original disclosure.

The appellant argues, in reliance upon Weste, that Vss is the lowest voltage available on the chip (brief, page 5). Weste states that "[t]he symbol '0' will be assumed to be a low voltage

[1] A rejection of claims 23-29 under 35 U.S.C. § 112, second paragraph, is withdrawn in the examiner's answer (page 3).

that is normally set to zero volts and called GROUND (GND) or $V_{SS}$" and that "[t]he power supplies ($V_{DD}$ and $V_{SS}$) are the source of the strongest '1's and '0's." Other sources indicate that Vss often means negative supply or ground, but that its meaning is determined by its usage.[2] Whether Vss always is the lowest voltage available on the chip is questionable in view of Momohara's disclosures that VSS can be ground potential and that a P-well can be biased with negative voltage VBB (col. 9, lines 32-33; col. 10, lines 39-40).

Regardless, even if Vss is the lowest voltage available on the chip, the record does not indicate that the appellant had possession of a circuit in which a P-well is biased by a bias potential above Vss. The appellant argues that "[t]he specification states that by varying the bias applied to the P-well, the performance of the device may be improved and that by using a higher bias potential on the P-well, better high frequency performance can be achieved. Necessarily, then, the

[2] *See* "CMOS Logic", in "*Application-Specific Integrated Circuits*" (Addison Wesley Longman 1997), http://www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/Book/CH02/CH02.htm; "Vcc, Vdd, Vss, etc.", wysiwyg://main.20/http://encyclobeamia.solarbotics.net/articles/vxx.html; "Electronic Symbols", http://www.control.com/1026184337/index_html. Copies of these references are provided to the appellant with this decision.

bias must be above the lowest voltage power supply bias that is available on the chip which is $V_{SS}$" (brief, page 5). What the specification states is (page 20, lines 9-13): "In some cases the lower frequency performance may also be improved merely by varying the bias ($V_A$) applied to the P-well 46. In other words, the higher the bias potential applied to the P-well 46, the better the high frequency performance." As pointed out by the examiner (answer, page 8), this disclosure pertains to the embodiment in figure 4 wherein the P-well is below inductor 50 and component 48 which appears to be a second inductor.[3] The appellant's claim 23, however, requires that a P-well below a logic circuit element (205; figure 19) is biased by a bias potential above Vss. The specification does not indicate that the disclosed benefit of increasing the bias to a P-well below inductors applies to biasing a P-well below a logic circuit element.

We therefore find that the appellant's original disclosure would not have conveyed with reasonable clarity to those skilled in the art that, as of the filing date sought, the appellant was in possession of a P-well biased by a bias potential above Vss.

[3] Component 48 is not identified in the appellant's specification.

Accordingly, we affirm the rejection under 35 U.S.C. § 112, first paragraph.

*Rejections under 35 U.S.C. § 103*

Momohara discloses an integrated circuit comprising a substrate having formed thereover a logic circuit element (processor 2) and an analog circuit element (7) (figure 22A). There is no dispute as to whether Momohara's disclosure of an analog circuit element would have fairly suggested, to one of ordinary skill in the art, the appellant's radio frequency element. The logic circuit element and the analog circuit element are above separate triple wells, each triple well being a P-well formed in an N-well in the P-substrate (figures 7 and 24).[4] Both P-wells are biased by "low potential power VSS (ground potential)" (col. 9, lines 31-33; col. 21, lines 35-37).

The examiner argues that "[o]ne has to guess the correlation [in the appellant's original disclosure] between the disclosed potential bias Va and the claimed potential bias Vss. Thus, appellant's inadequacies in disclosing the relationship between bias potential Va and the claimed bias potential Vss, render the bias potential of Momohara as being identical to Va and above

[4] The discussion of the processor in figures 6 and 7 (col. 9, lines 18-54) reasonably appears to apply to the processor in figure 22.

Vss" (answer, page 5). This argument is not well taken because Momohara's disclosure regarding the P-well bias voltage is not influenced in any way by the appellant's disclosure. Thus, any inadequacies in the appellant's disclosure are not capable of rendering Momohara's P-well bias potential as being above Vss.

The examiner argues that Momohara's disclosure that the P-wells are biased with "low potential power VSS (ground potential)" means that the P-wells can be biased with a low positive voltage while Vss is ground potential, and that the P-well can be biased with ground potential while Vss is a low negative voltage (answer, pages 8-9). In either of these cases, the examiner argues, the P-well is biased with a bias potential above Vss. *See id.* Even if Momohara's disclosure that the P-wells are biased with "low potential power VSS (ground potential)" means that Vss can be either ground potential or a low potential other than ground potential, Momohara does not disclose that the P-well bias voltage can be one of these potentials while Vss is the other of them. Instead, Momohara indicates that the P-well is biased with whichever of these potentials is Vss. Hence, Momohara does not teach that the P-well bias voltage can be greater than Vss.

For this reason and because the examiner has not provided evidence or reasoning which shows that one of ordinary skill in the art would have modified Momohara's integrated circuit such that the P-well is biased with a bias potential above Vss, the examiner has not carried the burden of establishing a *prima facie* case of obviousness of the appellant's claimed integrated circuit. Accordingly, we reverse the rejections of claims 23-29 under 35 U.S.C. § 103.[5]

[5] The examiner does not rely upon Zhu for any disclosure that remedies the above-discussed deficiency in Momohara.

*DECISION*

The rejection of claims 23-29 under 35 U.S.C. § 112, first paragraph, written description requirement, is affirmed. The rejections under 35 U.S.C. § 103 of claims 23-29 over Momohara and claim 25 under 35 U.S.C. § 103 over Momohara in view of Zhu are reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

*AFFIRMED*

| | | |
|---|---|---|
| Terry J. Owens<br>Administrative Patent Judge | ) | |
| Peter F. Kratz<br>Administrative Patent Judge | ) | BOARD OF PATENT<br>APPEALS AND<br>INTERFERENCES |
| Catherine Timm<br>Administrative Patent Judge | ) | |

TJO/eld

Timothy N. Trop
Trop, Pruner & Hu, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024-1805